7th Symposium on Frequency Standards and Metrology Summary Submission for Invited Oral Presentation

CSAC – The Chip-Scale Atomic Clock

R. Lutwak[*] and A. Rashed – Symmetricom
M. Varghese[**], G. Tepolt, J. LeBlanc, and M. Mescher – Charles Stark Draper Laboratory
D.K. Serkland, K.M. Geib, and G. M. Peake – Sandia National Laboratories

Robert Lutwak – RLutwak@Symmetricom.com

Atomic frequency standards play an essential role in the synchronization and accuracy of modern timing, communications, and navigation systems. To date, however, the relatively large size and power consumption of conventional technologies have prevented their deployment in portable, battery-powered applications. Over the past decade, advances in micro-electromechanical systems (MEMS), low-power semiconductor lasers, low-power microwave electronics, and battery technology, along with improved understanding of the physics of atomic vapor samples in miniature cells, have opened the possibility of a new generation of atomic clocks, 100X smaller and lower power than conventional technologies. Low-power chip-scale atomic clocks (CSACs) enable new capabilities in diverse applications, including secure communications and ad hoc networking, remote sensor networks, and high-integrity navigation.

At the time of the 6th FSM, one research group, from NIST, reported on research on small low-power atomic oscillators[1]. Today, seven years later, and due in large part to significant investment by the U.S. Defense Advanced Research Projects Agency (DARPA), more than two score academic and industrial laboratories worldwide are involved in CSAC research and development. Successful CSAC development requires collaborative development of state-of-the-art technologies from diverse specialties, including micro-elecromechanical systems (MEMs), optoelectronics, low-power electronics, and firmware algorithms.

The authors have been developing CSAC technology since 2001. Throughout the project, emphasis has been placed on autonomy, reliability, and robustness, in order to facilitate rapid system-level integration and capability demonstration. We demonstrated our first prototype in the Spring of 2005 with power consumption ≈ 150 mW and short-term stability of $\sigma_y(\tau)<6\times10^{-10}\tau^{-1/2}$ [2]. In 2007, we completed a pre-production build and evaluation of 10 identical CSACs, with power ≈ 125 mW, and short-term stability of $\sigma_y(\tau)<2\times10^{-10}\tau^{-1/2}$ [3].

This paper will describe the architecture, construction, and performance of the Symmetricom CSAC, review the statistical results of the pre-production build, and present recent performance results. Prospects for further improvements in performance and power consumption will be discussed.

---

[*] Oral Presentation
[**] now at MEMSIC Inc. Andover, MA
[1] J. Kitching, et al. in *"Proceedings of the 6th Symposium on Frequency Standards and Metrology,"* p. 167.
[2] R. Lutwak, et. al. in *"Proceedings of the 2005 International Frequency Control Symposium*, p. 752.
[3] R. Lutwak, et. al. in *"Proceedings of the 2007 International Frequency Control Symposium*, p. 1327.